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**CLAIMS:****1. (Currently amended)**

An integrated circuit, comprising logic circuits connected to a plurality of shift register latch scan chains and self-test circuits for testing said logic circuits, said self-test circuits in said integrated circuit comprising:

a pseudo random pattern generator for generating at least one flat pseudo random patterns to provide to each of the scan chains;

a plurality of weighting circuits for receipt of the pseudo-random patterns from the pattern generator, a different one of the weighting circuits associated with each of the scan chains, each weighting circuit having for providing a selectable weight set to provide [[said]] flat or weighted pseudo random patterns to the scan chains independently of one another;

a different storage element associated with each of the weighting circuits for receipt and storage of [[a]] flat and weighted pseudo- random patterns each from [[the]] its different associated random pattern generator weighting circuit; and

a selection circuit for individually addressing each of the storage elements for providing said selective entry of either a flat or weighted pseudo random pattern [[to]] into different shift register latches of said scan chains independently of one another for scanning said weighted pattern to said logic circuits to enable provision of pseudo-random patterns of different weights to the storage elements different shift register latches in the same scan chain.

**2. (Original)**

An integrated circuit as recited in claim 1, wherein said weighting circuit comprises a weight generating circuit and a weight selecting circuit.

SN 10/055,275

8

POU920000057US1

## 3. (Original)

The integrated circuit as recited in claim 1, wherein said weighting circuit includes means for receiving a weighting instruction from an external source to said integrated circuit.

## 4. (Original)

The integrated circuit as recited in claim 1, wherein said storage elements are each a first stage of an associated scan chain.

## 5. (Currently amended)

The integrated circuit as recited in claim 4, wherein said pseudo random pattern generator and said weighting patterns, receipts pattern and weighting instructions are from a tester internal to said integrated circuit.

## 6. (Original)

The integrated circuit as recited in claim 4, wherein said weighting instruction is generated by a tester external to said integrated circuit.

## 7. (Original)

The integrated circuit as recited in claim 4, further comprising a memory or register array wherein at least a portion of said weighting instruction is stored in said memory array.

SN 10/055,275

9

APPENDIX - CLAIMS OF 11/26/2004

POU920000057US1

## 8. (Currently Amended)

A method of testing an integrated circuit, comprising logic circuits connected to multiple shift register latch scan chains and self-test circuits on said integrated circuit for testing said logic circuits, the method comprising:

- a) generating a flat pseudo random pattern in said integrated circuit by using a linear feedback shift register;
- b) providing having weight selection circuits in said integrated circuit for providing a weight to said pseudo random patterns independently for each of the scan chains; and
- c) having a selection circuit for selectively providing loading a different one of said flat or weighted pseudo random patterns into to at least one but not all the scan chains on a shift register latch by shift register latch basis for scanning said weighted pattern to the logic circuits.

## 9. (Currently amended)

The method as recited in claim 8, wherein said weighted pseudo random pattern is introduced to a portion but not all of said shift register latches in at least one scan chain while a flat pseudo-random pattern is introduced to other of the shift register latches of said at least one scan chain by the selection circuit.

## 10. (New)

The integrated circuit of claim 1, wherein said pseudo random pattern generator is a linear feedback shift register coupled to each of the weighting circuits to provide a flat pseudo random pattern to each of the weighting circuits.

APPENDIX - CLAIMS OF 11/26/2004

POU920000057US1

## 11. (New)

The integrated circuit of claim 10, wherein the scan paths contain multiple shift register latch stages  $SRL_1$  to  $SRL_m$  each with first and second stages which  $SRL$  stages are controlled by an A clock, a B clock, and a  $C_1$  clock.

## 12. (New)

The integrated circuit of claim 11, wherein the first shift register stage  $SRL$  of each scan chain functions as said storage element associated with the scan chain and received at its  $L_1$  latch an input from the associated weighting circuit, an address input from an address decoder of the selection circuit and a w-clock for separately addressing each of the scan paths to enable entry of data from an associated weighting circuit into the first stage of the scan path on a  $SRL$  by  $SRL$  of the scan path basis.

## 13. (New)

The integrated circuit of claim 12 including means performing the following loading sequence steps individually for each of the plurality of scan paths:

generating the next flat or weighted pseudo-random pattern;

applying the  $L_1$  scan clock (A-clk) to load all the  $L_1$  latches of the register array with flat or weight pseudo-random data from the LFSR;

updating an  $L_1$  in any specific  $SRL_1$  stage scan path by addressing the particular  $L_1$  latch stage and applying the w-clock;

loading the  $L_2$  latch from the  $L_1$  latch (B-clk); and

repeating all the steps until the longest scan chain is loaded.

SN 10/055,275

11

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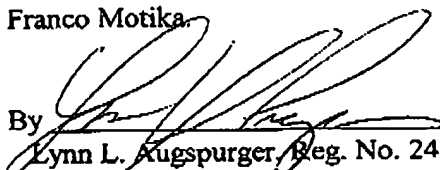
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Notice of allocane is now requested.

Respectfully Submitted,

15 For the Inventor(s):  
Franco Motika

By   
Lynn L. Augspurger, Reg. No. 24,227  
914-433-1174

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20

CERTIFICATE OF FACSIMILE UNDER 37 CFR 1.8(a) / UNDER 37 CFR 1.10

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25

Assistant Commissioner for Patents  
Washington, D.C. 20231

For Lynn L. Augspurger, Attorney of Record

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